# Wafer-Level Hysteresis-Free Resonant Carbon Nanotube Transistors

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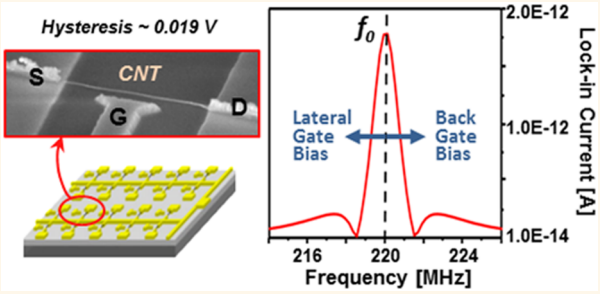
**ABSTRACT** We report wafer-level fabrication of resonant-body carbon nanotube (CNT) field-effect transistors (FETs) in a dual-gate configuration. An integration density of $>10^6$ CNTFETs/cm$^2$, an assembly yield of >80%, and nanoprecision have been simultaneously obtained. Through combined chemical and thermal treatments, hysteresis-free (in vacuum) suspended-body CNTFETs have been demonstrated. Electrostatic actuation by lateral gate and FET-based readout of mechanical resonance have been achieved at room temperature. Both upward and downward *in situ* frequency tuning has been experimentally demonstrated in the dual-gate architecture. The minuscule mass, high resonance frequency, and *in situ* tunability of the resonant CNTFETs offer promising features for applications in radio frequency signal processing and ultrasensitive sensing.




**KEYWORDS:** carbon nanotube · wafer-scale fabrication · nanoprecision · field-effect transistors · resonators · hysteresis-free · *in situ* tuning

Research in the fields of complementary metal-oxide-semiconductor (CMOS) and a nano-electromechanical system (NEMS) is growing rapidly, aiming at future miniaturized high-performance devices. Carbon nanotubes (CNTs), in particular single-walled (SW) CNTs, stand out as a promising candidate due to their unique physical, electrical, and mechanical properties associated with high integration density and surface-to-volume ratio.[1−3] Suspending CNTs, compared to the ones adhered to the substrate, offer many opportunities in chemical/bio/optical/displacement sensing,[2−6] as well as in electromechanical resonance based applications such as mass sensing, radio frequency (RF) signal processing, and single-device radios.[7−9] The miniscule CNT mass (attogram range), high eigenfrequencies, and potentially high quality factor $Q$[10] make CNT resonators suitable for atomic scale mass/force detection.[11] Meanwhile, the integrated field-effect transistor (FET) properties strongly facilitate resonant motion detection with low power consumption.[12,13] Further, frequency tunability of CNT resonators is important for parametric amplification schemes or communication applications. Currently, the actuation, resonance detection, and *in situ* frequency tuning of CNT resonators were typically demonstrated with a back gate.[8,14,15] However, the back gate configuration is not applicable for controlling and tuning individual CNT resonators in large arrays.

So far, the major challenge of manufacturing CNT-based devices has been large-scale high-precision CNT integration onto CMOS circuitry. It requires that each CNT is placed at a desired location with specified direction and density in a CMOS-compatible process. Two major approaches are involved in CNT assembly: controlled CNT synthesis and CNT assembly by postsynthesis techniques. Currently, chemical assembly[16] and solution-based precise assembly, *e.g.*, resist-assisted dielectrophoresis (DEP),[17] are the most precise techniques for CNT CMOS devices. For NEMS applications, efforts are needed to suspend CNTs without substrate etching, which may damage the nanotubes.[18] Besides, in a CMOS-compatible process, nanotube devices typically get contaminated, thus lack reproducible device properties, *e.g.*, gate hysteresis.[4,19−21] Although gate hysteresis may be useful in some cases such as memory cells,[22]

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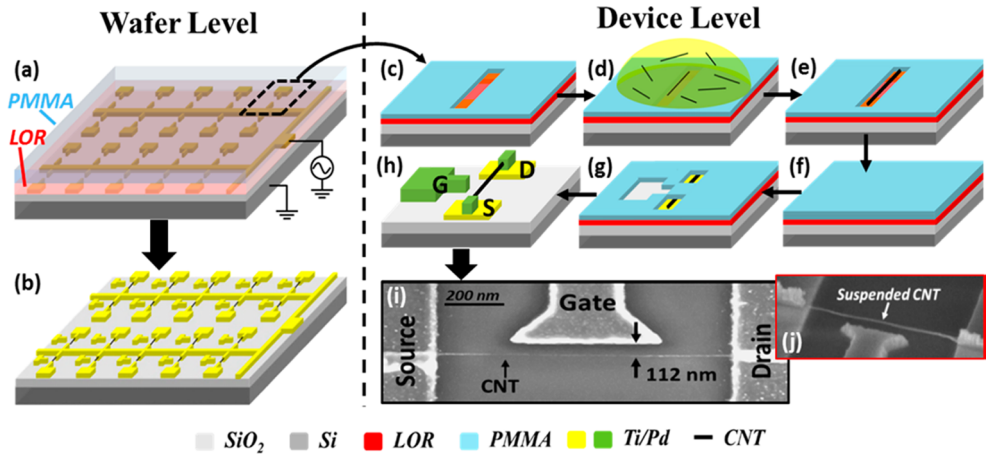


**Figure 1. Wafer-scale precise assembly of CNTFETs. (a, b) View of dense CNTFET arrays with a common guiding electrode during (covered by resists) and after processing. (c−h) Resist-assisted precise DEP integration of a CNTFET simultaneous with millions of others. (i) Scanning electron microscopy (SEM) of a typical CNTFET with straightened suspended CNT body showing little slack. The lateral gate is aligned with nanoscale precision and the side view (j).**

it has posed a persistent challenge in most electronic applications, resulting in inaccurate transport properties.[21]

To address these issues, we introduce a wafer-scale CNTFET fabrication scheme that combines the high precision of resist-assisted DEP technique[12] and the scalability of a capacitively coupled electrode method.[23,24] Individual access, high integration density, high yield, nanoprecision, and minimized contamination are the key advantages. The suspended CNTFETs exhibit negligible hysteresis in a vacuum. We electrostatically actuate individual suspended CNTFETs by lateral gates. Downward frequency tuning *via* the lateral gate and upward tuning *via* the back gate have been demonstrated. Tunable resonant CNTFETs are suitable for integration in a CMOS readout and desirable for RF signal processing and ultrasensitive sensing.

## RESULTS AND DISCUSSION

**Wafer-Level Assembly of Suspended CNTFETs.** A typical CNT lateral gate transistor fabricated by the wafer-level assembly technique as described in Materials and Methods is shown in Figure 1i, which represents the wafer-scale CNT array (Figure 1b). The suspended CNT channel is aligned to the desired position with nanoprecision, showing little slack or tension as well as negligible resist residue from the side view in Figure 1j. The lateral gate was aligned 112 nm away from the CNT body, ensuring strong gate−channel coupling for CNTFETs and electromechanical coupling for CNT resonators.

The statistical results from 10 wafers (Figure 2a) indicate that DEP duration plays a crucial role in precise CNT integration. When DEP duration is optimized (45 s in this work), on average, >80% guiding electrodes turned out to be spanned by one individual CNT or a small bundle (Figure 2b).

By the precise assembly technique, the suspended-body CNTFETs could be further scaled: the CNT channel length and the CNT−lateral gate distance could be brought arbitrarily close within EBL resolution; the guiding electrode area could be decreased according to the limitation of the capacitively coupled electrode scheme.[17,24] Estimated based on these geometrical limitations, an array consisting of 400 CNT devices can be fabricated simultaneously in a 100 $\mu$m × 100 $\mu$m area, giving a high density of 3−4 million nanotube transistors per cm$^2$. It is comparable to current ultra-large-scale integration (ULSI) complexity.[24]

The high-yield fabrication scheme featuring precisely controlled location, orientation, and shape of individual CNTs is promising for future commercialization of CNT-based devices.

**Static Electrical Characterizations.** Static measurements of the lateral-gate-suspended CNTFETs were performed in a high-vacuum probe station, Suess Microtech PMC 150. Base pressure is set below $10^{-6}$ Torr to exclude the influence of the charge traps originating from attached water molecules.

Figure 3 shows the transfer characteristics of the suspended CNTFET shown in Figure 1i. It operates as a laterally gated p-type FET. We obtained an $I_{on}/I_{off}$ ratio of $\sim 10^4$ at $V_{ds} = 0.3$ V and a subthreshold swing of SS = 220 mV/decade. The off currents ($I_{off}$) are at the detection limits of the measurement system (fA level). This indicates that the device has a very low or no leakage current, which is an important feature for low power consumption. The transfer characteristics suggest that the suspended CNT channel is effectively controlled by the lateral gate though a 112 nm air gap (vacuum). The on-state resistance could be greatly improved by further annealing the CNTFETs at higher temperature (600−800 °C) in a vacuum or forming gas.[25]

As shown in Figure 3, negligible gate hysteresis is observed in a vacuum when the gate bias is swept

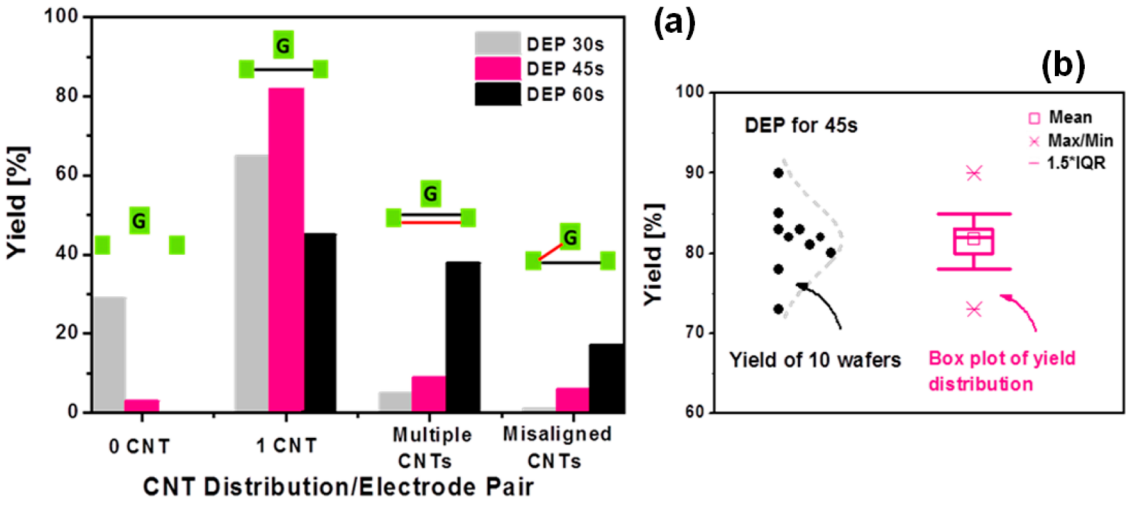


**Figure 2. (a) Histogram of yield of wafer-level precise CNT assembly technique (featuring one or one small bundle of CNT/electrode pairs) at different DEP duration. Insets: Possible failure including missing CNTs, multiple CNTs, and misaligned CNTs. (b) Box plot of the yields of 10 wafers processed by the CNT assembly technique at 45 s DEP duration. It shows the variation of the bridging yields (>80%). The max/min, mean, and 1.5IQR (interquartile ranged) values are shown.**

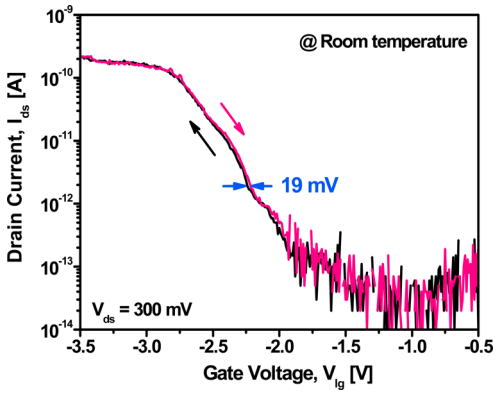


**Figure 3. Transfer characteristics of the suspended CNTFET (Figure 2i) in forward and backward sweeps at room temperature. Negligible hysteresis of the device with a clean CNT body is observed in a vacuum.**

forward and backward between −3.5 and −0.5 V. The hysteresis in gate voltage is as low as 0.019 V in a vacuum, and the hysteresis in current is 1 pA, which corresponds to 0.5% of $I_{on}$ (~0.2 nA). The hysteresis of our device is comparable with one of the best records (in vacuum) reported in the CNTFETs fabricated by resist-free CNT growth.[19,21] Negligible hysteresis here is believed to be a key advantage of the clean suspended CNT surface. Hence, the transfer characteristics have not been disturbed by charge traps originating from the substrate, the resist residue, the surfactant, or the water molecules on the surface of the CNT channel.

In general, gate hysteresis is attributed to the charging of traps that shield the CNT from the gate, thereby shifting the threshold voltage of the device. In conventional CNTFET fabrication, the CNT gets contaminated due to direct contact with the photoresist, which is used to define the contacts. The resist residue wrapping the CNT may fully/partially isolate the CNT channel from the gate, causing hysteresis. The complete removal of such contamination is challenging. Techniques, such as aggressive $O_2$ plasma used for semiconductor devices, could damage the CNTs. Moreover, in suspended CNTFET fabrication, the water molecules and the surfactant induced by the aqueous solution may get wrapped around the CNT channel by the resist residue and become the sources of charge traps. The contamination cannot be eliminated by simple annealing. In other words, the complex contamination consisting of resist residue, water molecules, and surfactant can influence the density of charge traps and hence the hysteresis.

Therefore, it is crucial to develop an efficient way to remove contamination without damaging the CNT channels.[26]

To investigate the effect of chemical and thermal treatments on gate hysteresis, we compared five sets of CNTFETs with various release and annealing conditions: resist removal temperature, release duration, and annealing conditions. Microposit Remover 1165 was used to dissolve the resists and release the devices. Annealing was performed under vacuum.

As shown in Figure 4a, all CNT channels in set 1 (released at 25 °C for 12 h; no annealing) are covered by a large amount of resist. In set 2 (released at 25 °C for 24 h; annealed at 200 °C for 1 h) (Figure 4b), typically, only a thin film of resist is left on the CNT surface.[27,28] The amount of resist in set 3 (released at 60 °C for 24 h; no annealing) is further reduced, leaving part of the CNT surface exposed without obvious resist coating (Figure 4c). In set 4[29] (released at 75 °C for 24 h; no annealing) and set 5 (released at 75 °C for 24 h; annealed at 200 °C for 1 h), the CNT channels of all samples appear to be very clean with hardly any resist residue (Figure 4d and e).

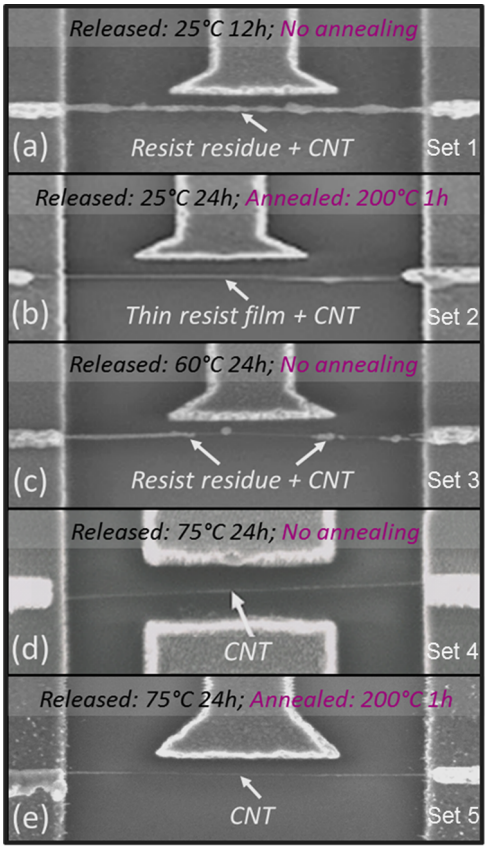


**Figure 4. Typical SEM images of the suspended CNTFETs with different release (with Microposit Remover 1165) and annealing (in a vacuum) conditions: (a) released at room temperature for 12 h, no annealing; (b) released at room temperature for 24 h, annealed at 200 °C for 1 h; (c) released at 60 °C for 24 h, no annealing; (d) released at 75 °C for 24 h, no annealing; (e) released at 75 °C for 24 h, annealed at 200 °C for 1 h. Obvious resist amount change can be observed.**

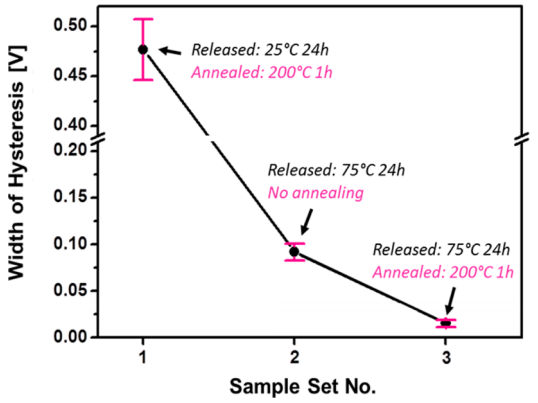


**Figure 5. Statistical data of the gate hysteresis of the suspended CNTFETs measured under vacuum (as shown in Figure 4b, d, and e) with different chemical/thermal treatments. Hysteresis reduction with optimized treatments in this work indicates minimized contamination on the CNT surface, ensuring high accuracy and resolution in sensing.**

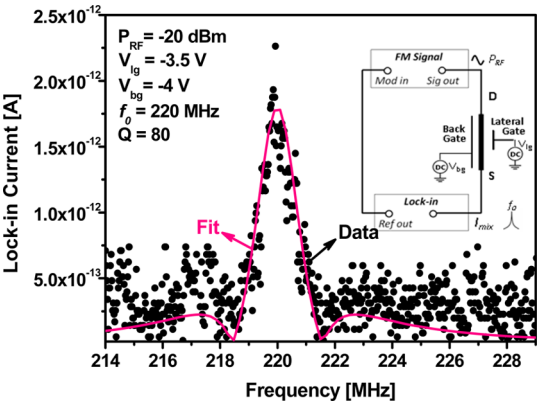


**Figure 6. (a) Transmission characteristic of the resonant CNTFET (750 nm long) measured at room temperature along with a Lorentzian fit. Inset: Frequency-modulated (FM) mixing measurement setup.**

The above experimental results imply that higher removal temperature and longer release duration give rise to the release efficiency.

We measured hysteresis characteristics of three sets (sets 2, 4, and 5) of CNTFETs at room temperature (RT) in a vacuum.

From the statistical data in Figure 5, one can see that the voltage width of the hysteresis gets smaller as the resist residue on the CNT surface diminishes. Two heavily contaminated CNTFETs as in set 2 (Figure 4b) show a relatively large hysteresis width, ~0.45 V. Hysteresis of the clean suspended CNTFET in set 4 (Figure 4d) decreases to ~0.09 V. Note that the gate hysteresis of the annealed CNTFET in set 5 (Figure 4e) has been significantly reduced to ~0.019 V (Figure 5). The dramatic decrease in gate hysteresis proves that (1) a higher release temperature helps to dissolve the resist, thus less contamination is left on the CNT surface to provide charge traps, and (2) the annealing step effectively eliminates the water molecules and absorbates on the exposed CNT channel; hence the hysteresis is suppressed.

**CNT Resonator Characterizations.** Suspended CNTFETs with good performance serve as a solid basis for detecting the mechanical resonance of the CNTs using FET-based readout. The mixing current for the resonant CNTFET at RT is shown in Figure 6 with $V_{lg}$= −3.5 V and back gate bias $V_{bg}$= −4 V. A good Lorentzian fit to the experimental data was obtained. The resonance frequency $f_0$ was extracted to be ~220 MHz, and a quality factor $Q$ of ~80 was obtained. A very low background noise floor (<5 × $10^{-13}$A) has been observed as expected in our low-leakage CNTFETs by the frequency-modulated (FM) technique,[30] which made it possible to detect the ultralow mixing current (2.3 × $10^{-12}$A).

Generally, gate-induced frequency tuning of NEM resonators is attributed to two mechanisms:[31] (1) the capacitive softening effect, which decreases the resonance frequency due to the nonlinearity of the electrostatic force; and (2) the elastic hardening effect, which increases the resonance frequency due to the increased beam tension.

In conventional back-gated CNT resonators, CNT motions are perpendicular to the electric field direction,

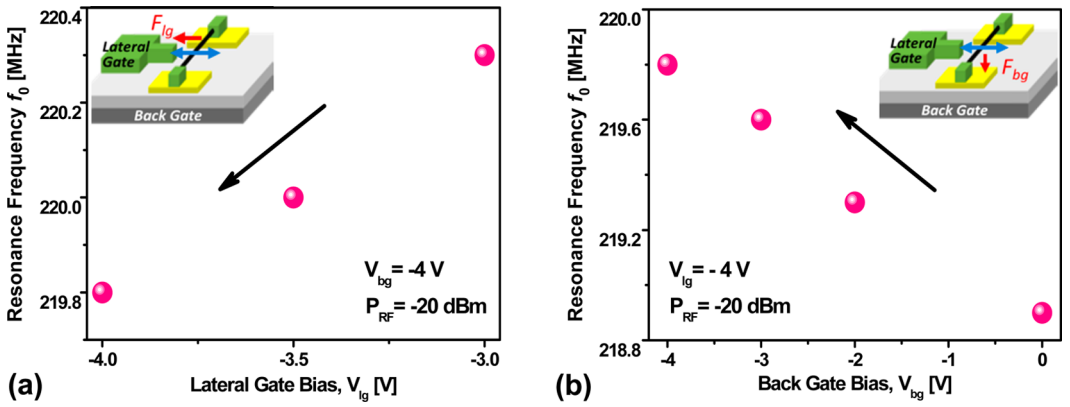


**Figure 7. (a) Downward resonance frequency tuning of the resonant CNTFET by the lateral gate at room temperature. (b) Upward resonance frequency tuning of the same resonant CNTFET by the back gate at room temperature. Insets: Schematics of the resonant CNTFET in two tuning modes.**

resulting in negligible capacitive softening. However, our dual-gate configuration (lateral and back gates) and narrow gate−CNT gaps offer opportunities to tune the resonant frequency *in situ* with more freedom.

The ac signal applied to the drain terminal introduces flexural motion inside the lateral electrode plane (the "in-plane" mode). When $V_{lg}$ is applied, the electrostatic force $F_{lg}$ is in the direction of the CNT motion. Therefore, both tension and a capacitive softening effect are created. Figure 7a shows that the resonant frequency $f_0$ shifts downward as $V_{lg}$ increases. A frequency tuning of ~0.2% by a $V_{lg}$ variation of 1 V was obtained. The net effect of $F_{lg}$ appears to be softening the effective spring constant, which reduces $f_0$.

On the other hand, when $V_{bg}$ is applied to the back gate, the electrostatic force $F_{bg}$ is perpendicular to the CNT motion and only induces tension by pulling the CNT toward the back gate. Therefore, an increase of $V_{bg}$ provides elastic hardening, which gives rise to $f_0$ (Figure 7b). The resonance frequency can be tuned ~0.1% by a $V_{bg}$ variation of 1 V. Here, low $V_{lg}$ and $V_{bg}$ were applied in case the CNT got destroyed.

*In situ* upward and downward tuning have been demonstrated within the same CNT resonator configuration. For both tuning modes, the tuning efficiencies are considered good for CNT resonators operating at these resonance frequencies.[11,12] The dual-gate configuration and upward/downward frequency tunability give more freedom for RF communication design where the center frequency of the filter can be fine-tuned. Besides, the individually addressable tunable CNT resonators in arrays can serve as sensing pixels, which make a large-scale sensor network feasible.

Figure 8 displays the resonance response of a resonant CNTFET with a 1 $\mu$m channel at 77 K. The resonance frequency was extracted to be ~126.5 MHz, and the quality factor $Q$ has been greatly improved to ~135. In our case, the CNT body length is on the same order of magnitude with the acoustic phonon mean

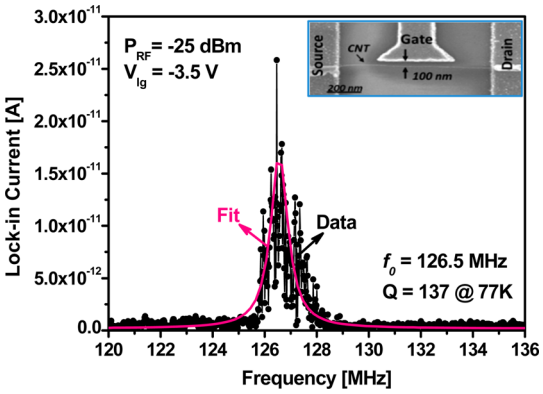


**Figure 8. (a) Transmission response of a resonant CNTFET (1 $\mu$m long) measured at 77 K along with a Lorentzian fit. Inset: SEM of the measured suspended CNTFET.**

free path (0.5−1 $\mu$m). Higher $Q$ may be associated with lower temperature $T$ due to the thermoelastic effect ($Q^{-1} \sim T^2$).[12] Clamping losses, surface effects, and contamination from processing could also influence the dissipation.

Due to very low mass and atomic structure, CNTs are ideal for ultra-high-resolution sensing. With further optimization of the readout and quality factor, such resonant CNTFETs could provide a mass detection noise floor at the zg level, which is interesting for ultra-high-resolution mass sensing.[32]

## CONCLUSION

In conclusion, we report wafer-scale suspended CNTFET fabrication with high precision, yield, and density as well as negligible hysteresis under vacuum. Lateral gate electrostatic actuation and FET-based detection of the resonant CNTFETs have been achieved at RT. Thanks to the dual-gate configuration (lateral and back gates), the resonance frequency of the resonant CNTFETs can be tuned *in situ* either upward or downward at RT. These results provide valuable insight into the future commercialization of CNT-based

NEMS systems for ultrasensitive mass sensing and RF communications. The suspended-body structures also serve as the basis for more complex digital and non-digital applications.

## MATERIALS AND METHODS

**Wafer-Level Fabrication of Suspended CNTFETs.** The assembly of SWCNTs was performed under ambient conditions. The CNT suspension was prepared using commercially available SWCNTs (SG 65i) purchased from SWeNT Inc. (Supporting Information).

Figure 1a–h show the schematic of the electrode arrangement at wafer level (Figure 1a,b) and the detailed assembly process at the device level (Figure 1c–h).

Guiding electrode pairs and alignment markers were patterned on a $SiO_2$ (500 nm)/Si substrate (Figure 1a). In this setup, for each guiding electrode pair, one electrode was connected to a common electrode (labeled as "ce"), and the floating one (labeled as "fe") was capacitively coupled to the underlying substrate (back electrode, labeled as "be"). Between each "ce–fe" electrode pair, a 30 nm wide trench was transferred to the resist layers (100 nm LOR/50 nm PMMA) by e-beam lithography (EBL) (Figure 1a and c).

The ac signal was applied between the common electrode and the silicon substrate for 45 s (Figure 1a and d). Individual SWCNTs in solution were simultaneously attracted and aligned into each trench (Figure 1e). For high electric-field frequencies (>100 kHz), "fe" electrodes are capacitively coupled to the substrate, which allows grounding all "fe" without probing them one by one.

CNT clamps and lateral gates were precisely defined on a second PMMA layer by EBL and deposited by metal lift-off (Figure 1f,g). Resists were stripped in Microposit Remover 1165 at 75 °C for 24 h, and slack was minimized by critical point drier (Figure 1b and h). Annealing at 200 °C in a vacuum for 1 h was applied. The suspension height is adjustable by the LOR thickness.

*Conflict of Interest:* The authors declare no competing financial interest.

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*Supporting Information Available:* Details of (a) CNT suspension preparation; (b) output characterization; (c) lateral gate tuning; (d) back gate tuning; (e) static characterization at 77 K. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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